Docket No.: 043876-0144 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: 4587
Application No.: 10/616,303	:	Group Art Unit: 2676
Filed: July 10, 2003	:	Examiner: Mackly Monestime

For: PROGRAMMABLE PROCESSOR AND METHOD WITH WIDE OPERATIONS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (REFERENCES)

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BOX 1 OF 5

OIPE IAP96 JAN 03 2006 PATENT & TRADEMARK OFFICE

OIPE IAP96 JAN 03 2006 PATENT & TRADEMARK OFFICE

Docket No.: 43876-144 **PATENT**

IFW CD-Rom

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: 4587
Application No.: 10/616,303	:	Group Art Unit: 2183
Filed: July 10, 2003	:	Examiner: Mackly Monestime

For: PROGRAMMABLE PROCESSOR AND METHOD WITH WIDE OPERATIONS

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Information Disclosure Statement in the above-identified application.

☐ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☒ Also attached: Form 1449 and cited references (in hard copy and CD/ROM), Notice of Concurrent Proceedings

☒ Please charge my Deposit Account No. 500417 in the amount of $180.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Kenneth L. Cage
Registration No. 26,151

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 KLC/jam
Facsimile: 202.756.8087
Date: January 3, 2006

Please recognize our Customer No. 20277 as our correspondence address.

OIPE IAP56
JAN 03 2006
PATENT & TRADEMARK OFFICE

Docket No.: 043876-0144 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: 4587
Application No.: 10/616,303	:	Group Art Unit: 2676
Filed: July 10, 2003	:	Examiner: Mackly Monestime

For: PROGRAMMABLE PROCESSOR AND METHOD WITH WIDE OPERATIONS

NOTICE OF CONCURRENT PROCEEDINGS

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Please be advised of the following concurrent reexamination proceedings, which involve related patents to the above-identified matter:

Control No.	**Patent No.**
90/007,531	5,809,321
90/007,532	6,584,482
90/007,563	5,794,061
90/007,583	5,742,840
90/007,593	5,794,060
95/000,089	6,643,765
90/007,618	6,269,136
90/007,634	5,737,547
90/007,647	5,336,926

90/007,758 5,985,692
95/000,100 6,725,356

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Kenneth L. Cage
Registration No. 26,151

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 KLC:jam
Facsimile: 202.756.8087
Date: January 3, 2006

OIPE IAP96
JAN 03 2006
PATENT & TRADEMARK OFFICE

Docket No.: 043876-0144 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Craig HANSEN, et al.	:	Confirmation Number: 4587
Application No.: 10/616,303	:	Group Art Unit: 2676
Filed: July 10, 2003	:	Examiner: Mackly Monestime

For: PROGRAMMABLE PROCESSOR AND METHOD WITH WIDE OPERATIONS

SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement, including completed Form PTO-1449, comprises a list of pertinent information of which Applicants are aware. A copy of each document listed on Form PTO-1449 is enclosed herewith.

The submission of this Information Disclosure Statement and the accompanying references is not an admission that the references cited are "prior art" with respect to the present invention, nor is it a representation that no better art exists. Applicants hereby reserve the right to swear behind or otherwise disprove any alleged "prior" nature of any art cited should the facts support and the situation warrant such an action.

Applicants write, in part, to disclose the settlement of litigation relevant to this reexamination. As reflected in the accompanying PTO Form 1449 and attachments, on March 26, 2004 MicroUnity Systems Engineering, Inc. ("MicroUnity") filed suit against Dell, Inc. and

01/04/2006 HALI11 00000133 500417 10616303
01 FC:1806 180.00 DA

Intel Corp. ("Intel") in the Eastern District of Texas alleging infringement of eight United States patents including United States Patent Nos. 6,643,765 B1 ("the '765 Patent") and 6,725,356 ("the '356 Patent"). *See* References A & B attached to PTO Form 1449. Subsequently, on April 15, 2005, Intel submitted a petition for *inter partes* reexamination of the '765 Patent and '356 Patent, which the PTO granted and which is currently pending. The '356 patent is in the priority chain of the present application. The '356 Patent is a continuation of patent 6,295,599, which is the parent of the '765 Patent. A Notice of Concurrent Proceedings of reexamination proceedings is also being submitted in a separate paper. The '765 Patent and '356 Patent are among eight patents now being asserted against Sony Entertainment for alleged infringement in the Eastern District of Texas.

As reflected in the attachments to the accompanying PTO Form 1449, the litigation between MicroUnity and Intel relating to the '765 Patent has now settled. Although the settlement agreement itself is confidential, publicly available information (including Intel's own press release) reflects that Intel has agreed to pay $300 million for, among other things, a license under the '765 Patent. According to one New York Times article:

> Intel announced that it had settled a patent suit brought last year by MicroUnity. Of the $300 million to be paid, $140 million was charged against earnings in Intel's most recent quarter.
>
> The deal assures Intel of access to MicroUnity technology, which is used in Intel's current family of Pentium chips, and to patents that MicroUnity has developed more recently. . . .
>
> The agreement covers features like . . . processing designs for handling video and audio data. . . .

See J. Markoff, "*Intel Settlement Revives a Fading Chip Designer*," THE NEW YORK TIMES (October 20, 2005) at (attached as Reference C to PTO Form 1449). An October 18, 2005 Intel press release similarly recognizes that Intel and MicroUnity "entered into a settlement agreement

that resolves a patent infringement case and provides certain rights for Intel customers." *See* Intel Announces Record Revenue of $9.96 Billion; EPS of 32 Cents Includes Legal Settlement that Lowered EPS By Approximately 2 Cents" (October 18, 2005) (attached as Reference D to PTO Form 1449).

This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee.

Please charge the processing fee under 1.17(p) of $180.00 to Deposit Account 500417. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Kenneth L. Page
Registration No. 26,151

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 KLC:jam
Facsimile: 202.756.8087
Date: January 3, 2006

Please recognize our Customer No. 20277 as our correspondence address.

OIPE IAP56 JAN 03 2006 PATENT & TRADEMARK OFFICE

PTO/SB/08a 07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U. S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	1	of	10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
	AE	US-4,959,779	09/25/1990	Weber, et al.	
	AF	US-5,081,698	01/14/1992	Kohn	
	AG	US-5,113,506	05/12/1992	Moussouris, et al.	
	AH	US-5,155,816	10/13/1992	Kohn	
	AI	US-5,161,247	11/03/1992	Murakami, et al.	
	AJ	US-5,179,651	01/12/1993	Taaffe, et al.	
	AK	US-5,231,646	07/27/1993	Heath, et al.	
	AL	US-5,233,690	08/03/1993	Sherlock, et al.	
	AM	US-5,241,636	08/31/1993	Kohn	
	AN	US-5,280,598	01/18/1994	Osaki, et al.	
	AO	US-5,487,024	01/23/1996	Girardeau, Jr.	
	AP	US-5,515,520	05/07/1996	Hatta, et al.	
	AQ	US-5,533,185	07/02/1996	Lentz, et al.	
	AR	US-5,590,365	12/31/1996	Ide, et al.	
	AS	US-5,600,814	02/04/1997	Gahan, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where RelevantPassages or Relevant Figures Appear	T[6]
	AT	WO 93/11500				

Examiner Signature		Date Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard St.16 if possible. 6 Applicant is to place a check mark here if English language translation is attached. The collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing ,and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** ***If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2***

PTO/SB/08b (07-05)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	10/616,303
				Filing Date	July 10, 2003
				First Named Inventor	Craig Hansen
(use as many sheets as necessary)				Group Art Unit	2676
				Examiner Name	Mackly Monestime
Sheet	2	of	10	Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
	AW	Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 –848)	
	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767)	
	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)	
	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621)	
	BA	i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn	
	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)	
	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455)	
	BD	Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924)	
	BE	Lee et al., "MediaStation 5000: Integrating Video and Audio," IEEE Multimedia pp. 50-61 (Summer 1994) (51056DOC000901 – 912)	
	BF	TMS320C80 (MVP) Parallel Processor User's Guide, Texas Instruments (March 1995) (51056DOC003744 – 4437)	
	BG	TMS320C80 (MVP) Master Processor User's Guide, Texas Instruments (March 1995) (51056DOC000925 – 957)	
	BH	Bass et al., "The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 12-22 (April 1995) (51056DOC059283 – 289)	
	BI	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 – 282)	
	BJ	Gwennap, "New PA-RISC Processor Decodes MPEG Video: Hewlett-Packard's PA-7100LC Uses New Instructions to Eliminate Decoder Chip," Microprocessor Report, pp. 16-17 (January 24, 1994) (51056DOC002140 – 141)	
	BK	Gwennap, "Digital MIPS Add Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 – 459)	
	BL	Kurpanek et al., "PA7200: A PA-RISC Processor with Integrated High PerformanceMP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156)	
	BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167)	
	BN	Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	3	of	10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code [2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	BO	US-5,636,351	06/03/1997	Lee	
	BP	US-5,721,892	02/24/1998	Peleg, et al.	
	BQ	US-5,734,874	03/31/1998	Van Hook, et al.	
	BR	US-5,758,176	05/26/1998	Agarwal, et al.	
	BS	US-5,768,546	06/16/1998	Kwon	
	BT	US-5,887,183	03/23/1999	Agarwal, et al.	
	BU	US-5,996,057	11/30/1999	Scales III, et al.	
	BV	US-6,425,073	07/23/2002	Roussel, et al.	
	BW	US-6,516,406	02/04/2003	Peleg, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number [4] Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where RelevantPassages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard St.16 if possible. 6 Applicant is to place a check mark here if English language translation is attached. The collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing ,and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

PTO/SB/08b (07-05)
Approved for use through 07/31/2006. OMB 0651-0032.
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	10/616,303
				Filing Date	July 10, 2003
				First Named Inventor	Craig Hansen
(use as many sheets as necessary)				Group Art Unit	2676
				Examiner Name	Mackly Monestime
Sheet	4	of	10	Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
	BZ	Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 – 590)	
	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141)	
	CB	PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 – 176)	
	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776)	
	CD	Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 – 751)	
	CF	Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 – 763)	
	CG	Nikhil et al., "*T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 – 476)	
	CH	Papadopoulos et al., "*T: Integrated Building Blocks for Parallel Computing," ACM, pp. 624-35 (1993) (51056DOC007278 – 289)	
	CI	Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 – 262)	
	CJ	M. Phillip, "Performance Issues for 88110 RISC Microprocessor," IEEE, 1992 (51056DOC008752 – 757)	
	CK	M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 – 789)	
	CL	R. Mueller, "The MC88110 Instruction Sequencer," Northcon, 1992 (51056DOC009735 – 738)	
	CM	J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 – 742)	
	CN	K. Pepe, "The MC88110's High Performance Load/Store Unit," Northcon, 1992 (51056DOC009743 – 747)	
	CO	J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 – 063)	
	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 – 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 – 656)	
	CS	Awaga et al., "The μVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
	CT	Takahashi et al., "A 289 MFLOPS Single Chip Vector Processing Unit," The Institute of Electronics, Information, and Communication Engineers Technical Research Report, pp. 17-22 (May 28, 1992) (51056DOC009798 – 812)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

PTO/SB/08b (07-05)

Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	10/616,303
				Filing Date	July 10, 2003
				First Named Inventor	Craig Hansen
(use as many sheets as necessary)				Group Art Unit	2676
				Examiner Name	Mackly Monestime
Sheet	5	of	10	Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 – 194)	
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607)	
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)	
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279)	
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	
	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)	
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 – 607)	
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 – 918)	
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)	
	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)	
	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)	
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510)	
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443)	
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459)	
	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299)	
	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	6	of	10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666)	
	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 – 717)	
	DX	Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 – 710)	
	DY	Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 – 094)	
	DZ	Kohn et al., "A New Microprocessor with Vector ProcessingCapabilities," Electro/89 Conference Record, pp. 1-6 (April 11-13, 1989) (5156DOC070672 – 678)	
	EA	Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 – 642)	
	EB	Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 – 336)	
	EC	Margulis, "i860 Microprocessor Architecture," Intel Corporation (1990) (51056DOC066610 – 7265 and 5156DOC069971 – 70626)	
	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 – 700)	
	EE	Patel et al., "Architectural Features of the i860 – Microprocessor RISC Core and On-Chip Caches," IEEE, pp. 385-90 (1989) (5156DOC070679 – 684)	
	EF	Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 – 647)	
	EG	Perry, "Intel's Secret is Out," IEEE Spectrum, pp. 22-28 (April 1989) (5156DOC070648 – 654)	
	EH	Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 – 101)	
	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 – 427)	
	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 – 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 – 73027)	
	EQ	Hansen, "Architecture of a Broadband Mediaprocessor," IEEE COMPCON 96 (February 25-29, 1996) (MU0013276 – 283 and 51057DOC001825 - 831)	
	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 – 630)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 7 of 10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	ES	Arnould et al., "The Design of Nectar A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 – 923)	
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 – 040)	
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 – 300)	
	EW	Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 – 645)	
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, http://www.cs.wisc.edu/condor/doc/Wisc1dea.html (1993) (51056DOC068704 – 711)	
	EY	Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 – 929)	
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
	FA	Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)	
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 – 673)	
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662)	
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028)	
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)	
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 – II-524 (April 1994) (51056DOC003070 – 073)	
	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 – 327)	
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 – 942)	
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)	
	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 – 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)	
	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)	
	FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 – 942)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

PTO/SB/08b (07-05)

Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 8 of 10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 – 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 – 957)	
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 – 896)	
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 – 946)	
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 – 609)	
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)	
	FV	Toyokura et al., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipelined Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, pp. 74-75 (1994) (51056DOC003659 – 660)	
	FW	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 – 443)	
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256)	
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 – 936)	
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2m)," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 – 410)	
	GA	Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 – 655)	
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)	
	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)	
	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers	
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243)	
	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

PTO/SB/08b (07-05)

Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 9 of 10

Complete if Known	
Application Number	10/616,303
Filing Date	July 10, 2003
First Named Inventor	Craig Hansen
Group Art Unit	2676
Examiner Name	Mackly Monestime
Attorney Docket Number	43876-144

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	
		Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005	
	GT	The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005	
	GU	USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005	
	GV	The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005	
	GW	The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005	

Examiner Signature		Dated Considered	

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
043876-0144	**10/616,303**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **July 10, 2003**	GROUP: **2676**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A	US	6,643,765	11-04-2003	Hansen et al.	
	B	US	6,725,356	04-20-2004	Hansen et al.	
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				
		US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
	D	Intel Press Release, "Intel Announces Record Revenue of $9.96 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.